WE CLAIM AS OUR INVENTION:

1. (Amended) A semiconductor structure comprising:

a substrate having a device feature formed thereon;

a dielectric layer disposed over said substrate and device feature and having at least one contact hole formed therein;

a polish stop layer disposed over the dielectric layer and extending within the contact hole;

a layer of ~~tungsten~~metal disposed over the polish stop layer within the contact hole and forming a plug; and

wherein said polish stop layer comprises ~~one of~~ titanium aluminum nitride ~~(TiAlN) and titanium carbon nitride (TiCN)~~.

2. (Amended) The semiconductor structure of claim 1 and including a metal coating under said dielectric layer, said metal coating comprising a compound of titanium nitride ~~TiN~~ and aluminum.

3. (Amended) The semiconductor structure of claim 2 wherein the dielectric comprises a silicon ~~dioxide (SiO_2)~~oxide.

4. The semiconductor structure of claim 3, wherein the metal coating comprises an anti-reflective coating.

5. (Amended) The semiconductor structure of claim 1, wherein the ~~barrier~~polish stop layer comprises titanium aluminum nitride~~TiAlN~~ with between about 5 and 20 percent by weight of aluminum.

~~6. The semiconductor structure of claim 1, wherein the barrier layer comprises TiCN with between about 5 and 20 percent by weight of carbon.~~

7. The semiconductor structure of claim 2, wherein the metal coating comprises about 5 to 20 percent by weight of aluminum.

~~8. A chemical mechanical polish (CMP) stop layer for use in a semiconductor manufacturing process comprising one of titanium aluminum nitride (TiAlN) and titanium carbon nitride (TiCN) disposed over an underlying substrate for stopping a CMP process from compromising the underlying substrate.~~

~~9. The CMP stop layer of claim 8, further comprising TiAlN having between 5 and 20 percent by weight of aluminum.~~

~~10. The CMP stop layer of claim 8, further comprising TiCN having between 5 and 20 percent by weight of carbon.~~

~~11. A plasma etch stop layer for use in a semiconductor manufacturing process comprising titanium aluminum nitride (TiAlN) disposed over an underlying layer for stopping an etch process from compromising the underlying layer.~~

~~12. The plasma etch stop layer of claim 11, further comprising TiAlN having between 5 and 20 percent by weight of aluminum.~~

~~13. A method of forming a metal interconnect in a semiconductor device, the method comprising:~~

~~depositing a dielectric layer over a substrate;~~

~~forming a contact hole in the dielectric layer;~~

~~depositing a polish stop layer comprising one of titanium aluminum nitride (TiAlN) and titanium carbon nitride (TiCN) over the dielectric layer;~~

~~depositing a layer of metal over the polish stop layer and filling the contact hole;~~

~~exposing a top surface of the layer of metal to a chemical mechanical polishing (CMP) process to remove that portion of the layer of metal disposed over the dielectric layer and leaving a flat surface with the contact hole filled with a plug of the layer of metal, the polish stop layer preventing the CMP process from removing any portion of the dielectric layer.~~

~~14. The method of claim 13, further comprising depositing the polish stop layer to have between about 5 and 20 percent by weight of aluminum.~~

~~15. The method of claim 13, further comprising depositing the polish stop layer to have between about 5 and 20 percent by weight of carbon.~~

~~16. The method of claim 13, further comprising removing at least a portion of the polish stop layer by exposing the polish stop layer to a chlorine-containing plasma etch that is selective to the underlying dielectric layer.~~

~~16. A method of forming a microelectronics device, the method comprising:~~
~~disposing a layer of metal over a substrate;~~
~~depositing an etch stop layer comprising titanium aluminum nitride (TiAlN) over the layer of metal;~~
~~depositing a dielectric layer over the etch stop layer;~~
~~forming a patterned photoresist layer on the dielectric layer;~~
~~using an etch process to remove those portions of the dielectric layer exposed through the photoresist layer pattern; and~~
~~wherein the etch process is stopped by the etch stop layer so that no portion of the layer of metal is removed.~~

~~17. The method of claim 16, further comprising depositing the etch stop layer to comprise TiAlN having between 5 and 20 percent by weight of aluminum.~~

19. A semiconductor structure comprising:

a substrate layer;

a dielectric layer disposed over the substrate layer and having a via formed therein;

a polish stop layer comprising titanium nitride alloyed with carbon deposited over the dielectric layer and extending into the via;

a metal layer deposited over the polish stop layer and filling the via; and

wherein the polish stop layer has a hardness which is 30 to 35 percent greater than a hardness of titanium nitride alone for protecting the dielectric layer from a chemical mechanical polishing process used to remove a portion of the metal layer deposited outside of the via.

20. The semiconductor structure of claim 19, wherein the polish stop layer comprises titanium nitride alloyed with between 5 and 20 percent by weight of carbon.

21. A semiconductor structure comprising:

a metal layer disposed on a substrate;

a layer of titanium aluminum nitride disposed on the metal layer;

a dielectric layer disposed on the layer of titanium aluminum nitride;

a patterned layer of photoresist disposed on the dielectric layer exposing a selected portion of the dielectric layer to an etching process;

wherein the layer of titanium aluminum nitride functions as an etch stop layer upon removal of the selected portion of the dielectric layer to prevent the etching process from compromising the underlying metal layer.